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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/084,614	02/28/2002	Scott Bierly	0918.0153C	1621
27896	7590	06/28/2005	EXAMINER	
EDELL, SHAPIRO & FINNAN, LLC 1901 RESEARCH BOULEVARD SUITE 400 ROCKVILLE, MD 20850			LU, JIA	
			ART UNIT	PAPER NUMBER
			2634	

DATE MAILED: 06/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/084,614

Applicant(s)

BIERLY ET AL

Examiner

Jia W. Lu

Art Unit

2634

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 28 February 2002.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-24 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-4 and 7-24 is/are rejected.
- 7) ☒ Claim(s) 5 and 6 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 28 February 2002 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
 2. Ascertaining the differences between the prior art and the claims at issue.
 3. Resolving the level of ordinary skill in the pertinent art.
 4. Considering objective evidence present in the application indicating obviousness or nonobviousness.
2. Claims 1, 22-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over US patent 3,986,123, in view of Japanese Patent 8222934, further in view of US patent 6,763,062.
 - a. Regarding claim 1, patent '123 discloses a modulator (fig 3, "DIS") in a transmitter (fig 2, "CLT"), a demodulator (fig 5, "DIS") in a receiver (fig 2, "CLR"), and a shared processor (fig 2, "ELT", described on column 4, lines 40-44 to be in an application that is incorporated in its entity) configured to receive signals from the modulator and signals going to the demodulator (fig 2) and adjusts the amplitudes and phases of the incoming and outgoing signals in order to reduce processing distortion (column 1, lines

56-61). While patent '123 does not teach power control, amplitude and phase adjustments are well known in the art to be directly related to power control (for example, see title abstract of JP 08222934). The modulating and processing of signals in the baseband is also well known in the art to be the most common and basic form used in transmission. While patent '123 does not teach the transmitting and receiving via phased array antenna, the art of steerable phased array antenna is well known in the art, as shown in patent '062 (figure 2, element 41). It would have been obvious for one ordinarily skilled in the art to use a processor described in patent '123 to adjust phase and amplitude elements in order to control composite antenna pattern in both uplink and downlink, to ensure low gain in the direction of interference and higher gain in the direction of transmission/reception (patent '062, fig 2).

- b. Regarding claims 22 and 23, since a modem by definition is a system which modulates and demodulates, and a transceiver is a system that transmits and receives, patent '123 is both a modem and a transceiver.
3. Claims 2 and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over US patent 3,986,123 in view of Japanese Patent 8222934 and US patent 6,763,062 as applied to claim 1 above, and further in view of US patent 5,583,562.
- a. Regarding claim 2, although patent '123 does not show time-multiplexing of received data, the use of time-multiplexing in transceiver systems is

well known for their ability to increase the throughput of a communications resource (for example, patent '562, fig 1). It would have been obvious for one ordinarily skilled in the art to use time-multiplexing in a system described in 2 above in order to allow more users to use a single channel in a duplex system.

- b. Regarding claim 3, while patent '123 does not show the modulator to provide a time-multiplexed data stream from an input of multiple data streams, patent '562 shows a modulator (fig 1, element 130) receiving data symbols from a plurality of user channels (fig 1, element 110) and provide a single time-multiplexed data stream (column 5, lines 30-40). The reason to combine time-multiplexing with a modulator is stated in part a above.
4. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over US patent 3,986,123 in view of Japanese Patent 8222934 and US patent 6,763,062, further in view of US patent 5,583,562 as applied to claim 3 above, and further in view of US patent 6,768,458. While patent '123 does not show a modulator generating a plurality of modulated data in the time-multiplexed stream corresponding to a plurality of antenna elements, patent '458 shows a modulator (figure 5, elements 216 and 218) generating a plurality of modulated data symbols in the time-multiplexed stream, corresponding to a plurality of antenna elements (figure 5, element 250). It would have been obvious for one ordinarily skilled in the art for a modulating system described in patent '123 to time-multiplex a plurality of

modulated data symbols corresponding to antenna elements in order to increase directional gain in transmission.

5. Claims 7-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over US patent 3,986,123 in view of Japanese Patent 8222934 and US patent 6,763,062 as applied to claim 1 above, and further in view of US patent 6,831,943.

- a. Regarding claims 7-9, patent '123 does not describe the complex multiplication of signals in the processor relating to a plurality of user channels in a time-multiplexed manner. However, patent '943 teaches a transmission system where a processor unit (figure 10, elements 18 and 20) performs complex multiplication on signals on incoming signals that have been time-multiplexed (column 29, line 43), associated with a plurality of antennas (figure 1, elements A12). While the plurality of user channels is not shown, it is well known that a system using time-multiplexing takes signals from different users in order to multiplex them. It would have been obvious for one ordinarily skilled in the art to use complex multiplication in a system described in patent '123 for beamforming (column 7, lines 18-47) and power adjustments (column 15, lines 47-54) in order to improve power usage and reduce interference.
- b. Regarding claim 10, patent '123 does not disclose a beamformer configured to receive time-multiplexed baseband signals from shared baseband processor. Patent '943, however, shows a beamformer (figure 2, element 52) capable of receiving time-multiplexed (column 29, line 43)

signals from a front-end processor. It would have been obvious for one ordinarily skilled in the art to use a beamformer in a transceiver system described in patent '123 when incoming signals require directional and rotational adjustments in order to acquire precise directional transmission to increase gain while using lower power.

6. Claims 11-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over US patent 3,986,123 in view of Japanese Patent 8222934 and US patent 6,763,062 as applied to claim 1 above, further in view of US patent 6,549,527. While patent '123 does not show the front-end specifics of its receiving circuitry, patent '527 shows a plurality of down-converters (column 2, lines 29-33) separately down-converting signals for each antenna element (figure 14, element 142). It also teaches the down-converting circuitry to include decimation means (figure 1, element 11) followed by multiplexing means (figure 1, element 12). It would have been obvious for one ordinarily skilled in the art to use decimation and multiplexing in the receiver end in order enable signal processing in an antenna array system without lowering system performance or increasing price, dimension or complexity of the hardware (column 3, line 48-line 59).
7. Claims 14-16, 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over US patent 3,986,123 in view of Japanese Patent 8222934 and US patent 6,763,062 as applied to claim 1 above, further in view of US patent 5,809,422.
 - a. Regarding claims 14-16, while patent '123 does not show a demultiplexer and up-converters in transmission, patent '422 teaches the use of

demultiplexers (figure 4, element 134) and IF up-converters (column 7, lines 33-40) in separate transmitting antenna elements (column 11, lines 56-60). Patent '422 also teaches interpolation in order to increase the sampling rate of the transmission signals (column 13, lines 39-40). It would have been obvious for one ordinarily skilled in the art to employ demultiplexing in an transmission end as described in patent '123 in order to separate time-multiplexed symbols for transmission and up convert baseband signals into a higher, intermediate frequency in order to enable signal transmission in a wireless medium.

- b. Regarding claim 18, while patent '123 does not teach the use of TDMA, patent '422 teaches the use of TDMA (column 8, line 41) in its transceiver system. Because TDMA is a very common technique used in transmission, and it would have been obvious to one ordinarily skilled in the art to use TDMA to allow multiple users to share time slots within a single channel.
8. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over US patent 3,986,123 in view of Japanese Patent 8222934 and US patent 6,763,062 as applied to claim 1 above, further in view of US patent 5,937,348. While patent '123 teaches the use of a duplexer between the transmitter and receiver portion of its transceiver, it does not specify the duplex to be time-division or the use of a switch. Patent '348 shows a duplex switch capable of using time division duplex (column 5, line 20). It would have been obvious to one ordinarily skilled in the art

to use a switch in a time division duplex transceiver system described in patent '123 in order to provide better control over the system while allowing it to transmit and receive using a single front-end processor.

9. Claims 19-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over US patent 3,986,123 in view of Japanese Patent 8222934 and US patent 6,763,062 as applied to claim 1 above, further in view of US patent application 20020141478. While patent '123 does not show the use FDMA, FPGA or VLSI in its transceiver system, application '478 teaches all these elements (FDMA on paragraph 2, line 6, FPGA on paragraph 621, line 4, and ASIC on paragraph 621, line 5). It would have been obvious to one ordinarily skilled in the art to use FDMA to allow multiple users to share time slots, FPGA to increase flexibility in designs and programming, or ASIC to reduce power usage, save space and lower cost of production.

Allowable Subject Matter

10. Claims 5 and 6 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

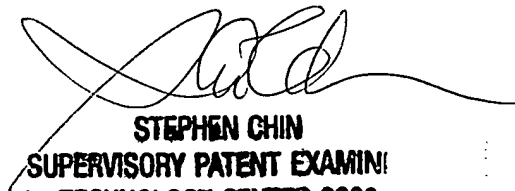
Art Unit: 2634

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jia W. Lu whose telephone number is 571-272-6042. The examiner can normally be reached on Mon- Fri, 10:30AM-6:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin can be reached on (571)272-3056. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jia Lu
Examiner



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